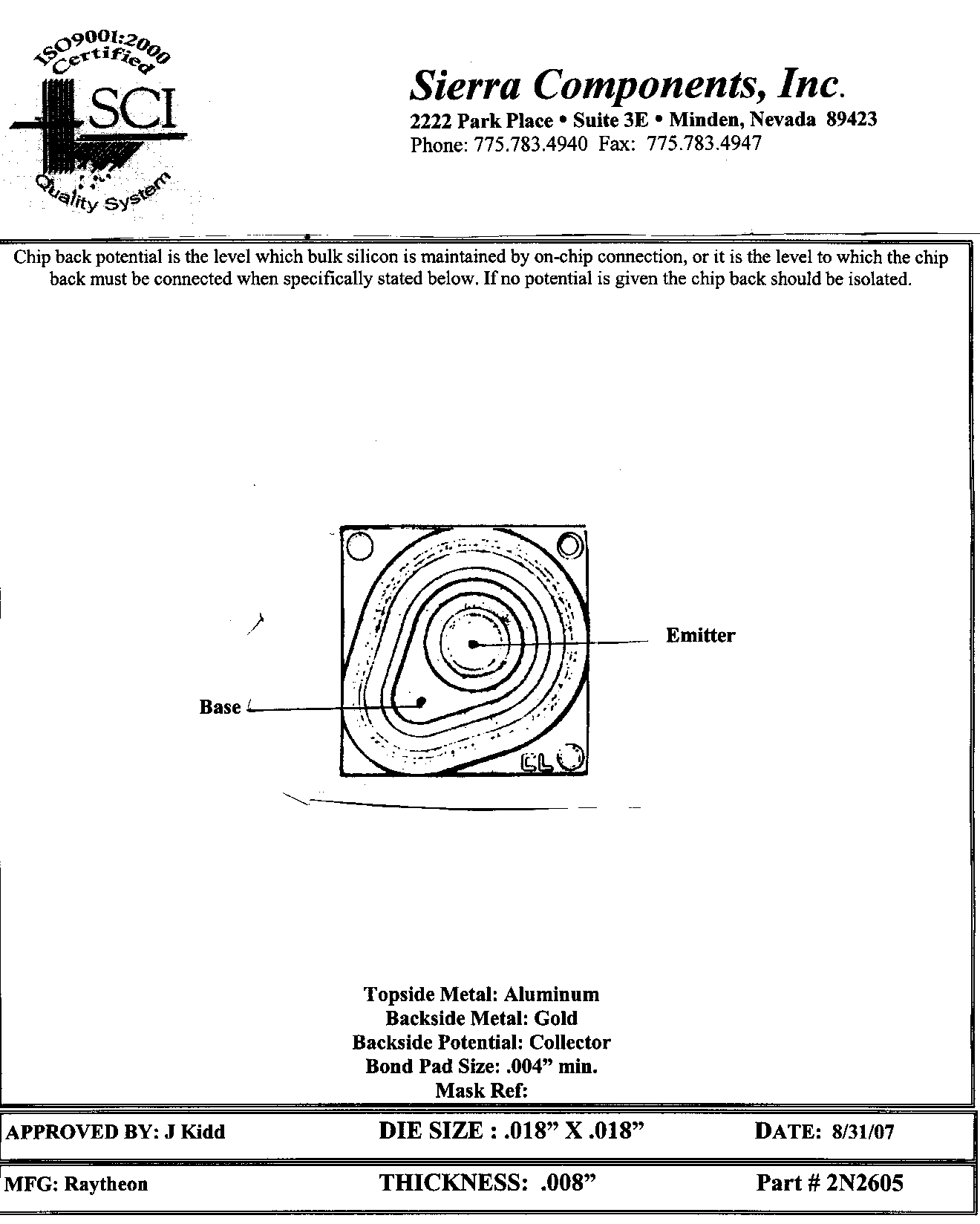
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**EMITTER**



**BASE**

**.018”**

**.018”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004 X .004” min.**

**Backside Potential: COLLECTOR**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .018” X .018” DATE: 1/26/22**

**MFG: RAYTHEON THICKNESS .008” P/N: 2N2605**

**DG 10.1.2**

#### Rev B, 7/1